Corner Analysis of Current Starved Sleep stack Voltage Controlled Oscillator With Phase Locked Loop for higher stability

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ABSTRACT:

This paper consists of a performance comparison of Current Starved Voltage Controlled Oscillator (CSVCO) for Phase Locked Loop (PLL). The work i.e. the design of Current Starved VCO is implemented using sleepy stack low power leakage technique. This has been implemented in 45nm CMOS Technology with a supply voltage of 0.45V in Cadence Software. The parameters like average power, oscillation frequency, and delay are calculated in different process corners showing the performance of improvement results of cadence simulation are reported. After comparison of the various parameters of PLL implemented with Sleep Stack CSVCO and Basic CSVCO, The sleepy stack approach is particularly useful in low power applications, The recommended PLL has a much smaller chip than previous designs, much lower power consumption and significantly higher efficiency. The proposed design of the PLL with Sleep Stack Technique makes the circuit efficiently to reduce sub-threshold leakage current, And achieves Frequency of 2.759 GHz, Power 2.559µw, phase noise -63.8(dBc/Hz) and Delay(µs) 0.0006544 respectively.

KEYWORDS: VCO, PLL, Gain, Gale-or, Lector, Control Voltage, Current Starved VCO, Oscillation frequency, Sleepy stack, Tuning Range.

1. INTRODUCTION

The Phase Locked Loop (PLL) is a control system used to generate the phase of output signal which is related to the phase of the input signal. The major blocks present in the PLL are Voltage controlled Oscillator and phase detector in a feedback loop. This paper depicts the one of the major blocks called VCO. The main functionality of the VCOs are in the communication systems. Among the multiple types of VCOs, the ring oscillators and LC oscillators plays a major role in terms of high frequency, less noise, wide tuning range [1]. and the area occupancy. The LC VCO which consists of an induct-or and capacitor occupies more area. The ring oscillators consist of the delay cells which have the same functionality similar to the buffer and these cells would occupy more area. In an ring oscillator, the last delay cell output is connected to the first delay cells input [2]. which is called as feed back .The delay cells can be either single ended or differential accordingly [4]. The increase in the number of delay cells give rise to consumption of area [6]. Because of the differences in the driving capability the characteristics of the VCO become nonlinear which can be avoided by adding feedback circuit. By adding this feedback circuit it further leads to the increase in cost of the circuit [7]. The current starved VCO technique was designed in order to overcome the disadvantages caused by the previous V CO's[7].

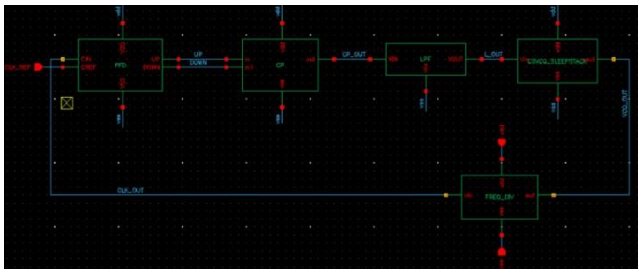

Fig.1. Schematic diagram for PLL with Sleep Stack Current Starved VCO

This paper is organized as follows. Section2 explains basic Current Starved VCO. Section 3 Describes different leakage power reduction techniques in CMOS Circuits. Section 4 Simulation result s and design comparisons. Finally Section5Concludesthis paper.

2. CURRENT STARVED RING VCO WITH SLEEP STACK & KEEPER TECHNIQUE

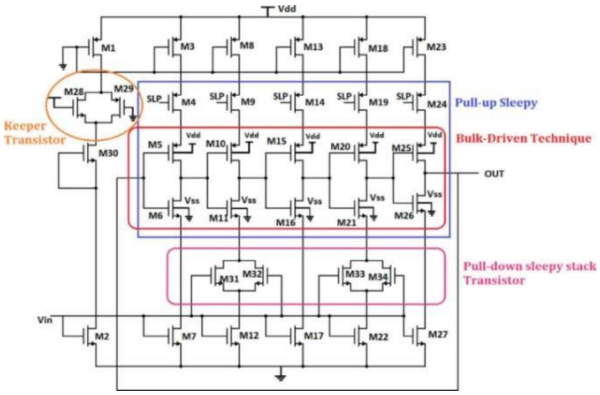

Fig.2. Current Starved Ring VCO with Sleepy stack & Keeper Technique Circuit

The sleepy stack approach is particularly useful in low-power applications or when power efficiency is a critical design consideration. It helps to reduce power consumption without sacrificing the speed or performance of the circuit. The purpose of the alternative arrangement in the proposed circuit is to reduce the no. of transistors and the area utilization. The alternative arrangement of the proposed design itself makes the circuit works efficiently to reduce sub-threshold leakage current, which in turn reduces power consumption. Therefore, not all the delay cells in the proposed design need to be connected with the sleepy stack approach.

3. CURRENT STARVED VCO PLL ARCHITECTURE WITH SLEEP STACK TECHNIQUE

Among the different types of V CO's, ring oscillator is the efficient in terms of frequency and driving capabilities. The ring VCO has been designed with delay stage. These delay stages further when increased lead to the non linearity of the circuit. This non linearity can be overcome by increasing the number of delay cells which has increased the complexity of the circuit and also increasing the power consumption [8]. The output frequencies of an basic VCO are controlled by the control voltage where as the current is controlled by the current starved VCO [9]-[10]. The circuit consists of delay cells along with the current mirror which is used to limit the current to all the delay cells. The current starved VCO alone together has also increased the leakages and power consumption [1]. These leakages can be further reduced by applying the low leakage techniques to the delay cells and by varying the aspect ratio of transistors which reduces the threshold voltage [11].

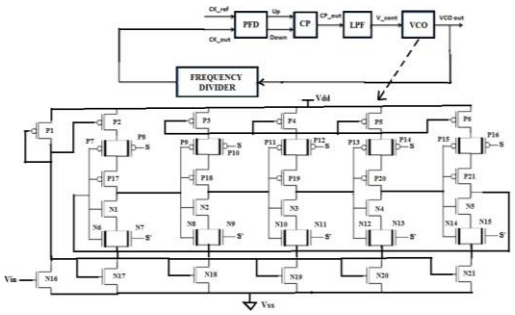

Fig. 3. PLL Architecture with current starved VCO

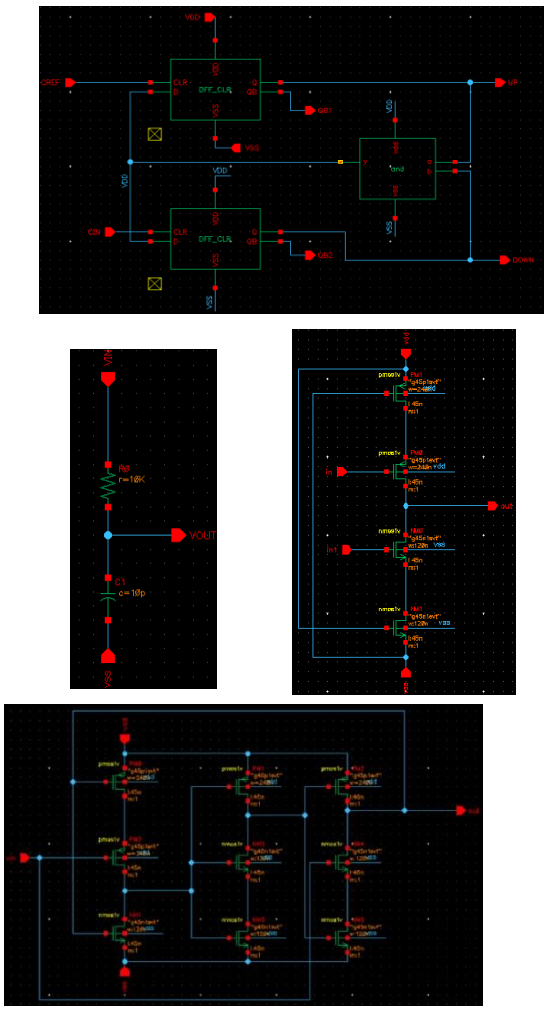

Fig. 3.1. PLL Internal blocks PFD, LPF, and CP & FD with CSVCO

The CSVCO circuit is implemented with sleep Stack technique, in which both the stack and sleep techniques are implemented above and below the pull up and pull down network respectively. In normal mode, the sleep transistor would go to sleep mode, then the stack transistors reduce the leakages [24-26]. In case of the active mode the sleep transistor becomes ON and stack transistors are OFF, reducing the leakages in CSVCO circuit.

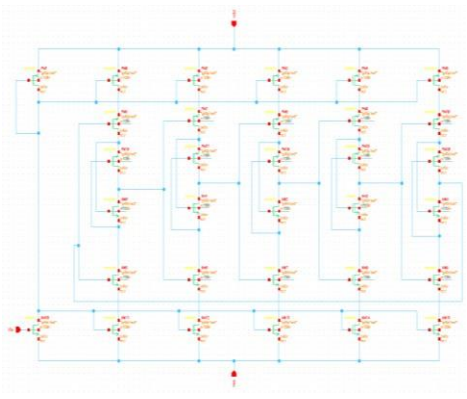

Fig.3.2. Schematic diagram for Current Starved VCO

3.1. LEAKAGE REDUCTION TECHNIQUES IMPLEMENTED IN CURRENT STARVED VCO

The basic CSVCO as shown in Figure 1 is operated with the input voltage namely control voltage (V_{ctrl}). As the V_{ctrl} decreases, the current that is to be mirrored from the transistorM1reduces when it is passed through the different PMOS in the delay stages. Because of the active mode of transistors in the CSVCO the leakage power has been increased [1].

In this paper, the current starved VCO has been implemented with different low power leakage techniques like Gale-or, Lector, Sleepy Keeper, Sleep, Stack and Sleepy Stack to observe the better performance of the circuit [12]. Performance analysis can be observed in terms of different parameters like frequency, delay and average power.

3.2. CURRENT STARVED VCO WITH GALE-OR TECHNIQUE

In the CSVCO circuit implemented with Gale-or technique as shown in Figure 2, has two high voltage transistors inserted between the pull up and pull down network whose gates are shorted to its self source terminals. These H Vt transistors form a stack there by reducing the leakages [14-15].

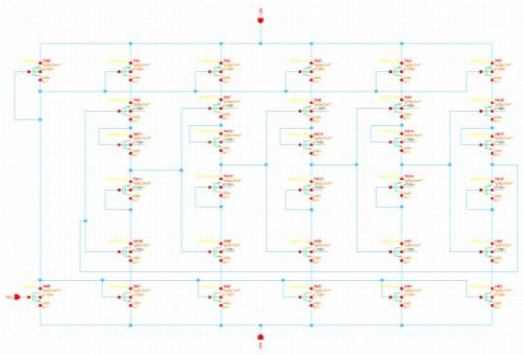

Fig.3.3.CSVCO using Gale-or Technique

3.3. Current Starved VCO with Lector Technique

In the CSVCO circuit implemented with lector technique as shown in Fig 3, two leakage control transistors are placed between the pull up and pull down network whose gates are controlled by the source of other transistors. By the introduction of LCTs, the resistance path from the power supply to ground is increased thus reducing the leakages without more additional circuits [16-17].

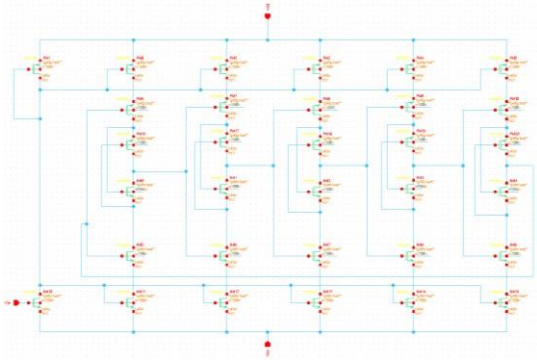

FIG.3.4. CSVCO USING LECTOR TECHNIQUE

3.4. CURRENT STARVED STACK VCO

The CSVCO circuit is implemented with Stack technique ueasshowninFigure4,in which the each transistor present in the pull up and pull down network of CSVCO is divided in to two equal parts and are placed one above the above which is called as stacking [20]-[21]. By stacking of these transistors the leakages can be reduced in each delay cell in different stages. The frequency and gain of the circuit would be increased based on the increase in the number of delay cell stages.

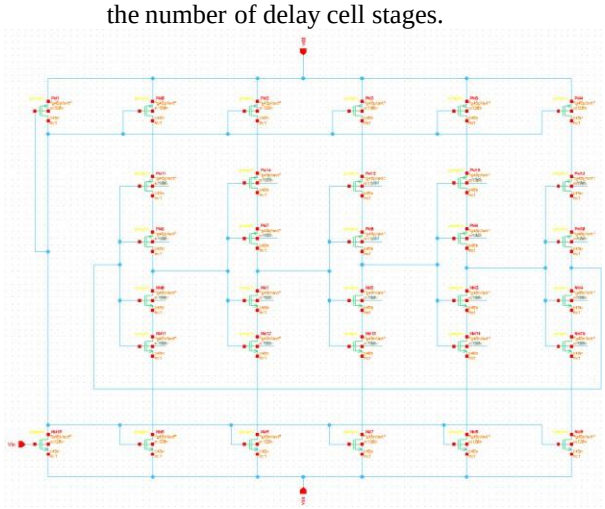

Fig.3.5. CSVCO using Stack Technique

The CSVCO circuit is implemented with Sleep technique as shown in Figure 5, in order to reduce the sub-threshold leakages by connecting either PMOS or NMOS transistors which are called sleep transistors [22]-[23]. The delay stages would operate in both the sleep mode also called as standby mode or in active mode. The sleep transistors would become OFF there by reducing the leakages.

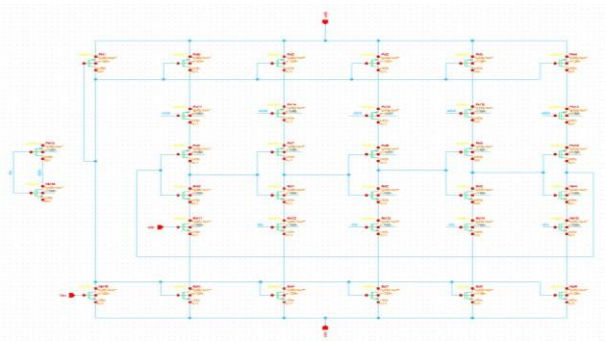

Fig.3.6. CSVCO using Sleep Technique

The CSVCO circuit is implemented with Stack technique as shown in Figure 6, in which both the stack and sleep techniques are implemented above and below the pull up and pull down network respectively. In normal mode, the sleep transistor would go to sleep mode,then the stack transistors reduce the leakages[24]-[26].

In case of the active mode the sleep transistor becomes ON and stack transistors are OFF, reducing the leakages in CSVCO circuit.

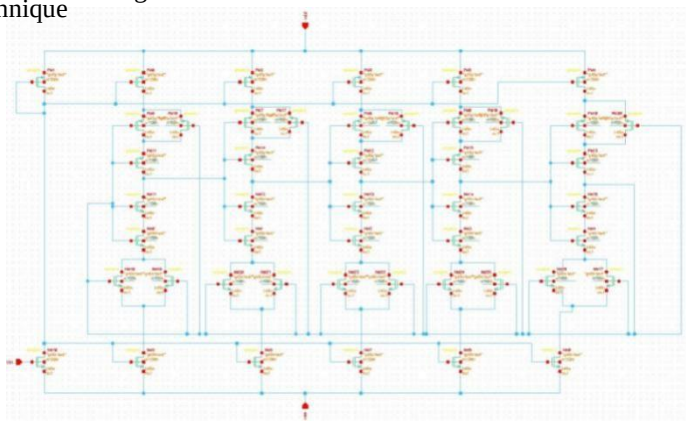

Fig. 3.7. CSVCO using Sleepy Stack Technique

4. PROCESS CORNER ANALYSIS

Corner analysis provides a convenient way to measure circuit performance while simulating a circuit with sets of parameter values that represent the most extreme variations in a manufacturing process. All the proposed circuits with different low leakage techniques have their average power, oscillating frequency and tuning range calculated in process corners like nominal, slow-fast, fast-slow, fast-fast and slow-slow conditions.

The mobility and the threshold voltage which in turn effect the device performance. if the threshold voltage is lowered then there is more current and effectively the device is faster however if the threshold voltage is increased there is less current and the device could be slower. A lower supply voltage causes slower switching of the gates and results into an overall slower circuit a high supply voltage drives faster switching of the larger gates which makes the circuits faster.

The process corner analysis in addition to temperature and voltage analysis is carried out with the Cadence Virtuoso tool using the 45 NM generic process design kit (GPDK) technology file. At 27℃ by representing a parallelogram as shown in below figure.

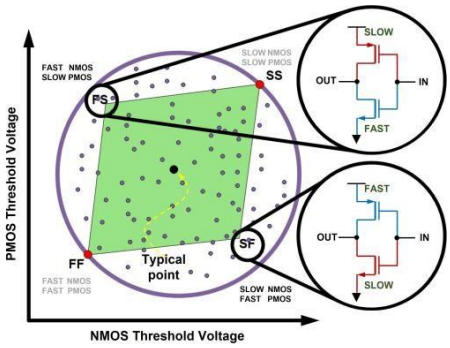

Fig.4. Process Corner variations in CMOS devices

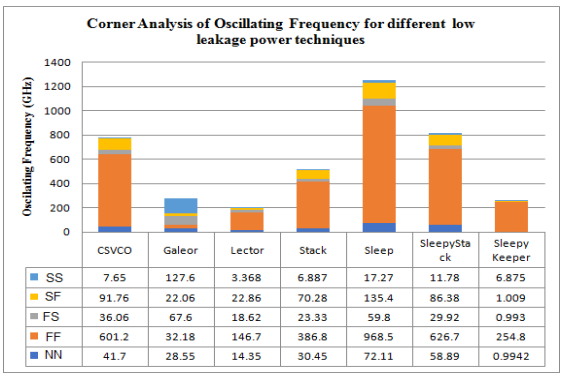

Fig.4.1. Corner Analysis of P_{avg} for CSVCO applied with different low leakage techniques.

From the above plotted graph it is observed that the average power in all the corners remained almost constant and in the Sleep Technique it is always less in all the corners.

From the below plotted graph it is observed that the oscillation frequency in all the corners remained less and in the Gale-or Technique it is very much reduced in all the corners.

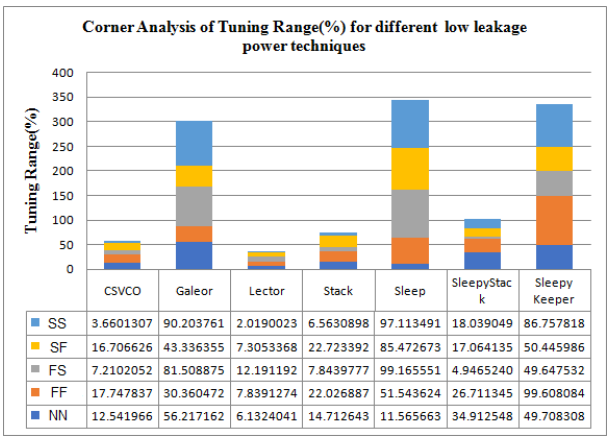

Fig.4.2. Corner Analysis of Oscillation Frequency(GHz) for CSVCO applied with different low leakage techniques.

From the below plotted graph it is observed that the frequency tuning range calculated in percentage for all the corners in case of Sleep technique remained high and in the Lector Technique it is very much reduced in all the corners.

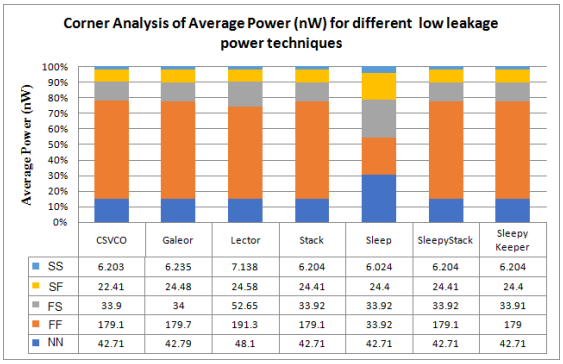

Fig.4.3. Corner Analysis plot of Frequency Tuning Range(%) for CSVCO applied with different low leakage techniques.

5. SIMULATION AND RESULT ANALYSIS

To analyse the circuit and to perform the simulation results of the CSVCO implemented different low leakage techniques, the circuits has been implemented in virtuoso tool in Cadence Software in 45nm Technology with a supply voltage of 0.45V.The simulated output of the oscillator is obtained by initializing setting the output node to either 1 or 0 to get the proper oscillations. The parameters like average power(P_{avg}),delay,Oscillation frequency and gain are calculated at a room temperature of27℃ and with a control voltage of 0.45V.

Table:1 Simulation results for Parameters with different low leakage power techniques in CSVCO

S. No.	Low Leakage Power Techniques	Average Power (W)	Area (μm2)	Delay (μs)	Frequency (GHz)	Gain (GHz/V)	Tuning Range (%)
1	Gale-or	48.20 e-9	37.5769	19.56	13.81	3.07	56.21
2	Lector	49.77 e-9	35.581225	32.25	14.34	3.19	6.07
3	Sleep	40.45 e-12	26.3169	327.8	72.11	16.02	98.76
4	Stack	49.56 e-9	56.4001	19.03	30.45	6.76	14.71
5	Sleep Stack	58.32 e-9	37.5769	0.4896	58.89	13.87	34.86

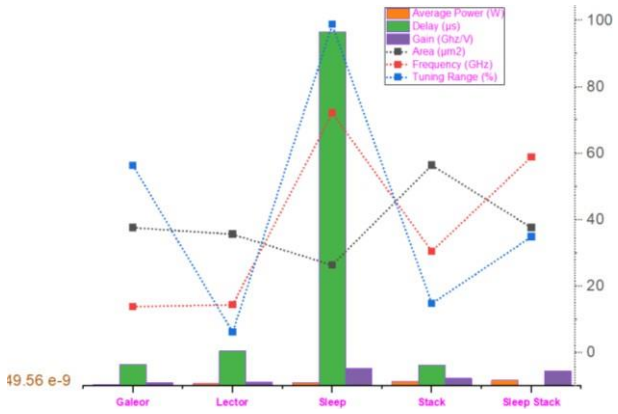

Fig.5. Parameter analysis of CSVCO with different low leakage power techniques

Table: 2 Comparison analysis of PLL CSVCO VS sleep stack PLL CSVCO

Parameters	PLL with basic CSVCO	Proposed work-PLL with SLEEP STACK CSVCO
VCO type	Ring	Ring
Tech(NM)	45	45
Freq(GHz)	2.592	2.759
Supply volt(v)	1	1
Power(MW)	0.002686	0.002559
P-Noise(dBc/Hz)	-72.2	-63.8
Delay(µs)	0.866	0.0006544

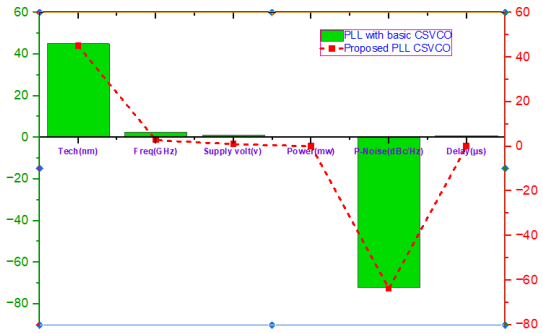

Fig. 5.1. Comparison analysis of PLL CSVCO & Sleep Stack PLL CSVCO

6. CONCLUSIONS AND FUTURE SCOPE

From the above tabular column and the graphs plotted it is observed that all the low leakage power techniques applied to the existing CSVCO are better in one or the other parameter like average power, oscillation frequency, delay and the gain. It is also observed that as the temperature is increased from corner analysis 27℃ to 80℃then the power and delay are increased and they are decreased when the temperature is decreasedto-40℃.

After comparison of the various parameters of PLL implemented with Sleep Stack CSVCO and Basic CSVCO it is observed that Sleep Stack has better performance. To achieve further higher frequencies vary the supply voltage and the number of stages in the CSVCO i,e from 5 stages to 7,9,11 and so on but with increase in other parameters like area and power.

REFERENCES

[1] Chandra Keerthi Pothina, C.K. Singh, N.P., Prasanna, J.L. Santhosh, (2023), Design of Efficient PLL for Low Power Applications, doi 10.3390/HMAM2-14157

[2] Saurabh Kumar ,R. K. Chauhan,(2023),Design of energy efficient VCO for PLL application Analog IC's & Signal Processing,doi.10.1007/s10470- 022-02122-y

[3] B.Meena Kumari, Goobala Kavya, (2023), Implementation of Digital Phase Locked International Journal of Engineering Technology and Management Sciences, DOI:10.46647/ijetms.v07si01.022 ISSN: 2581-4621

[4] Dina M. Ellaithy,(2023),Voltage-controlled oscillator based analog-to-digital

[5] converter in 130-nm CMOS for biomedical applications Journal of Electrical Systems & Information Technology volume 10.

[6] Arunkumar Pundalik Chavan, Ravish Aradhya, (2023), Design of 5.1 GHz ultra-low power and wide tuning range hybrid oscillator, oscillator doi.org/10.11591/ijece.v13i4,78-3787

[7] R Gurjar, DK Mishra, (2023), Design and performance analysis of low phase noise LC voltage controlled oscillator, doiorg/10.12928/telkomnika.v21i4.22341

[8] Dina Ellaithy,(2023),Voltage-controlled oscillator based analog-to-digital converter in 130-nm CMOS for biomedical applications DOI:10.1186/s43067-023-00109-x

[9] Pooja Thool, J.D Dhande, Y. A. Sada warte, (2022), A Review on Design and Analysis of Low Power PLL for Digital Applications and Multiple Clocking Circuits (IJRASET) ISSN: 2321-9653.

[9] Nirmalraj, T, Radhakrishnan, S.,Karn, R. K,(2022),Design of low power, high speed PLL frequency synthesizer using dynamic CMOS VLSI technology.IEEE.

[11] Kalpana Kasilingam, Paulchamy Balaiyah, Piyush Kumar Shukla, (2022), Design of a high-performance advanced phase locked loop with high stability external loop filterdoi.org/10.1049/cds2.12130

[12] That Bao Phuc Ton,Cong Thinh Dang,(2022), A Design of 45nm Low Jitter Charge Pump Phase-Locked Loop Architecture for VHF and UHF Fields DOI: 10.21203/rs.3.rs-1804148/v1[4].B.

[13] S. DhanushT.N.Vaishnavi S. Parashar,(2021) Design and Implementation of High Frequency and Low-Power Phase-locked Loop, U.Porto Journal of Engineering DOI:10.24840/2183-6493_007.004_0006.

[14] Pawan Srivastava,Ram Chandra Singh Chauhan, (2021),Design of Power Efficient Phase Frequency Detector and Voltage Controlled Oscillator for PLL Applications in 45 nm CMOS Technology DOI:10.51201/JUSST/21/10879

[15] Vijay Kumar Sharma, (2021), A survey of leakage reduction techniques in CMOS digital circuits for nanoscale regime, Australian Journal of Electrical and Electronics Engineering, DOI: 10.1080/1448837X.2021.1966957

[16] Buddha Dharani, Umakanta Nanda (2021),Impact of Sleepy Stack MOSFETs in CSVCO on Phase Noise and Lock Performance of PLL, DOI:10.1007/s12633-021-01446-0

[17] Ayush Kumar Tiwari(2021),Leakage Power Reduction in CMOS VLSI Circuits using Advance Leakage Reduction Method, (IJRASET) DOI :10.22214/ijraset.2021.35065

[18] Prithiviraj R., Selvakumar J.(2021).Design and Analysis of Low power and High Frequency CurrentStarved Sleep voltage Controlled Oscillator for Phase Locked Loop Applications DOI:10.1007/s12633-020-00619-7

[19] Rekha Yadav;Usha Kumari; (2021). Design an optimal digital phase lock loop with current-starved ring VCO using CMOS technology . International Journal of Information Technology, doi:10.1007/s41870-020-00587-6

[20] MadhusudanMaiti, Suraj Kumar Saw, Abir Jyoti Mondal, Alak Majumder, (2020), A hybrid design approach of PVT tolerant, power efficient ring VCO doi.org/10.1016/j.asej.2019.10.009

[21] Nanda, U., Acharya, D. P., & Nayak, D. (2020). Process Variation Tolerant Wide-band Fast PLL with Reduced Phase Noise using Adaptive Duty Cycle Control Strategy.International Journal of Electronics. doi:10.1080/00207217.2020.1793414

[22] Santhosh Rani, M., Vinothkumar, K., Krishna moorthy, Jaya sankar, (2021). Design of low power VCO using Fin FET technology for biomedical applications.Materials Today:Proceedings,45,2145–2151. doi:10.1016/j.

[23] Kabirpour, Saeideh; Jalali, Mohsen (2019). A highly linear current-starved VCO based on a linearized current control mechanism. Integration, S0167926018303596 – . doi:10.1016/j.vlsi.2019.06.008

[24] Shirin Askari, Mohsen Saneei, (2018),Design and analysis of differential ring voltage controlled oscillator for wide tuning range and low power applications,doi.org/10.1002/cta.2582

[25] R.Prakash Rao,(2018), IMPLEMENTATION OF VARIOUS LOW POWER TECHNIQUES IN A CMOS SRAM CELL IJCRT Volume 6, Issue 2ISSN: 2320-2882

[26] Neha Pathak, Prof. Ravi Mohan(2014)Phase Locked Loop Design and Implementation using Current Starved Voltage Controlled Oscillator DOI : 10.17577/IJERTV3IS20745

[27] Malviya H, Nayar S, Roy C "A New Approach FOR Leakage Power Reduction Techniques in Deep Submicron Technologies in CMOS Circuit for VLSI Applications" Int J Adv Res Comput Sci Softw Eng. 3(5):318–25,2013.

[28] Barua 2012. "A novel architecture for nanometer scale low power VLSI design". In: 2012 15th International Conference on Computer and Information Technology (ICCIT). IEEE: 490– 4.

[29] Pal PK, Rathore RS, Rana AK, Saini G. "New low p Power techniques: Leakage feedback with stack & sleep stack with the keeper". In: 2010 International Conference on Computer and Communication Technology, ICCCT-2010. IEEE. 296–301.

[30] Jun Cheol Park, "Sleepy stack: a new approach to low power VLSI logic and memory", School of electrical and computer engineering , Georgia institute of technology , August 2005.